

What is claimed is:

- 1 1. A method of forming a gate for a FinFET comprising the steps of:
 - 2 forming a first mandrel over a substrate fin substantially perpendicular to the
 - 3 semiconductor fin, the mandrel having a first and second sidewalls perpendicular
 - 4 to the substrate;
 - 5 forming a first sidewall spacer on the first sidewall;
 - 6 removing the first mandrel;
 - 7 depositing a second mandrel over the substrate, the semiconductor fin and
 - 8 the first sidewall spacer;
 - 9 removing the first sidewall spacer thereby creating a first cavity extending
 - 10 through the second mandrel and exposing the semiconductor fin; and
 - 11 forming a first gate conductor within the first cavity.
- 1 2. The method of claim 1, further comprising the steps of:
 - 2 forming and a second sidewall spacer on the second sidewall;
 - 3 depositing the second mandrel over the second sidewall spacer;
 - 4 removing the second sidewall spacer thereby creating a second cavity
 - 5 extending through the second mandrel and exposing the semiconductor fin; and
 - 6 forming a second gate conductor within the second cavity.
- 1 3. The method of claim 2, wherein the step of forming the first sidewall spacer and
 - 2 the second sidewall spacer further includes the steps of:
 - 3 growing a first sidewall film on the first sidewall and a second sidewall film on
 - 4 the second sidewall;
 - 5 selectively removing portions of the first sidewall film thereby leaving the first
 - 6 spacer straddling the semiconductor fin; and
 - 7 selectively removing portions of the second sidewall film thereby leaving the
 - 8 second spacer straddling the semiconductor fin.

1 4. The method of claim 2, further comprising the step of:
2 forming respective gate dielectric material within the first and second cavities
3 on the exposed semiconductor fin, before forming the respective gate conductor in
4 each of the first and second cavities.

1 5. The method of claim 1, further comprising the step of:
2 removing the second mandrel.

1 6. The method of claim 2, wherein the step of depositing the second mandrel
2 further includes the step of planarizing the second mandrel to a height that exposes
3 the first and second sidewall spacers.

1 7. The method of claim 1, further comprising the step of:
2 forming a protective film on a top surface of the semiconductor fin.

1 8. The method according to claim 4, wherein the step of depositing respective gate
2 dielectric material further includes the step of:
3 removing any protective film within the first and second cavities before
4 forming gate dielectric material.

1 9. The method of claim 3, wherein the step of growing the first sidewall film and
2 second sidewall film include the step of growing each respective film to a thickness
3 equal to a desired channel length for the FinFET.

1 10. The method of claim 3, further comprising the step of:
2 removing any material that grows on a top surface of the first mandrel during
3 performance of the steps of growing the first and second sidewall films.

1 11. A semiconductor device fabricated according to a process comprising the steps
2 of:

3 forming a first mandrel over a substrate and a semiconductor fin
4 substantially perpendicular to the semiconductor fin, the mandrel having a first and
5 second sidewalls perpendicular to the substrate;

6 forming a first sidewall spacer on the first sidewall and a second sidewall
7 spacer on the second sidewall;

8 removing the first mandrel;

9 depositing a second mandrel over the substrate, the semiconductor fin and
10 the first and second sidewall spacers;

11 removing the first and second sidewall spacers thereby creating a first cavity
12 and a second cavity extending through the second mandrel and exposing the
13 semiconductor fin; and

14 forming a respective gate within each of the first and second cavities.

1 12. The semiconductor device of claim 11, wherein the process further comprises
2 the steps of:

3 growing a first sidewall film on the first sidewall and a second sidewall film on
4 the second sidewall;

5 selectively removing portions of the first sidewall film thereby leaving the first
6 spacer straddling the semiconductor; and

7 selectively removing portions of the second sidewall film thereby leaving the
8 second spacer straddling the semiconductor fin.

1 13. The method of claim 12, wherein the step of growing the first sidewall film and
2 second sidewall film include the step of growing each respective film to a thickness
3 equal to a desired channel length for the FinFET.

1 14. An intermediate structure formed during fabrication of a FinFET gate, the
2 intermediate structure comprising:

3 a planarized mandrel layer covering a semiconductor fin formed on a
4 substrate;

5 a first cavity extending vertically through the planarized mandrel layer thereby
6 exposing a first portion of the semiconductor fin and substrate, said cavity having
7 a width that determines a channel length of a first gate portion of the FinFET; and

8 a first gate conductor deposited within the first cavity.

1 15. The intermediate structure of claim 14, further comprising:

2 the semiconductor fin; and

3 a nitride cap formed over the semiconductor fin.

1 16. The intermediate structure of claim 14, further comprising:

2 a second cavity extending vertically through the planarized mandrel layer
3 thereby exposing a second portion of the semiconductor fin and substrate, said
4 cavity having a width that determines a channel length of a second gate portion of
5 the FinFET; and

6 a second gate conductor deposited within the second cavity.

1 17. The intermediate structure of claim 14, further comprising a gate dielectric
2 material separating the semiconductor fin and the first gate conductor.

1 18. The intermediate structure of claim 14, wherein:

2 the first cavity has a thickness substantially equal to an oxide sidewall spacer
3 grown on an oxide mandrel overtop of the semiconductor film.

1 19. The intermediate structure of claim 18, wherein:

2 the thickness is less than a feature size attainable using optical projection
3 lithography.